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09/722,049	11/27/2000	John Andrew Leonard	57761.000124	4434

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EXAMINER	
KLINGER, SCOTT M	

ART UNIT	PAPER NUMBER
2153	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/722,049	LEONARD, JOHN ANDREW	
	Examiner	Art Unit	
	Scott M. Klinger	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 8/24/2004

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-12 and 14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-12 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-5, 7-12, and 14-19 are pending.

Response to Arguments

Note: Applicant's remarks are in **bold** text. Examiner's responses are indented.

In particular, the features of claim 1 relate of manipulation of feedbacks and setpoints. The applied art fails to teach or suggest such claimed features, including, for example, "an interrupt line that transmits the interrupt signal and informs a communication processor connected on the main control card to update the feedbacks in the dual port memory and read the setpoints from the dual port memory," as claimed.

Applicant's arguments with respect to the rejection of claim 1 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made, see below.

It is respectfully submitted that based on the nature of Kerr, one would not have been motivated to combine the teachings of Kerr with GFK0728A. In short, Fig. 1 of Kerr relating to a TV tuner, a printer, 3D graphics and 3D audio appear reflective of the nature of Kerr. Such teachings of Kerr as described above, would not lead on of ordinary skill to utilize Kerr in GFK0728A, as proposed in the Office Action.

The Kerr describes data transfer of circuitry. Although the specific applications described in Kerr all refer to general consumer use, using the same types of circuitry in an industrial setting is not out of the scope of Kerr.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation *"the main control card"* on line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 8, 9, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over GFK-0728A (Programmable Controller IC697BEM763/764, 1 November 1995, hereinafter "GFK-0728A") in view of Kerr et al. (U.S. Patent Number 6,105,119, hereinafter "Kerr").

In referring to claim 1, GFK-0728A discloses an interface module that interfaces between drive systems and local area network (LAN) protocols. GFK-0728A shows an interface between a drive and a LAN (Figure 2, on page 3, shows a labeled drawing of the module). Although GFK-0728A shows substantial features of the claimed invention, GFK-0728A is silent as to the specific circuitry of the interface module. Nonetheless the circuitry for interfacing a drive to a LAN is well known in the art and would have been an

obvious modification to the system disclosed by GFK-0728A as evidenced by Kerr.

In analogous art, Kerr discloses data transfer circuitry that could be used to implement the system of GFK-0728A. In referring to claims 1, 8, and 15, Kerr shows,

- A dual port memory connected to a bus:

  "Generally, and in one form of the present invention, an integrated circuit includes a dual-port memory having a first memory port and a second memory port, a bus interface block including bus master and bus slave circuitry, and a byte-channeling block coupled between the first memory port and the bus interface block operable to convert non-aligned data into aligned data." (GFK-0728A, col. 3, lines 39-45)

- An ASIC:

  "The digital signal processor with an ASIC wrapper of this invention together provide super-bus-mastering to access the entire memory space in the system, including the entire virtual memory space accessible by the host processor." (GFK-0728A, col. 3, lines 49-53)

- An interrupt line:

  "FIG. 28A is an electrical circuit diagram of interrupt-related registers and interrupt lines to the PCI bus and to the DSP, used in process, device and system embodiments" (GFK-0728A, col. 5, lines 51-53)

- Control registers:

  "FIG. 38 is a DSP memory space diagram supplementing FIG. 36--right and showing DSP program, data and I/O spaces, including on-chip and off-chip memories and registers utilized in embodiments of processes, devices and systems herein" (GFK-0728A, col. 6, lines 17-21)

Given these teachings, a person of ordinary skill in the art would have readily recognized the desirability and advantages of using the data transfer circuitry of Kerr to implement the system of GFK-0728A, in order to permit drives to be controlled from application programs.

Although GFK-0728A in view of Kerr shows substantial features of the claimed invention GFK-0728A in view of Kerr does not show that the interrupt is used to update

feedbacks in the dual port memory and read the setpoints from the dual port memory. Nonetheless the use of feedbacks and setpoints is well known in the art and would have been an obvious use of the dual port memory disclosed by GFK-0728A as evidenced by Kerr. A person of ordinary skill in the art would have readily recognized the desirability and advantages of storing and reading feedbacks and setpoints, in order to control the drive.

In referring to claims 8 and 15, GFK-0728A discloses an interface module that interfaces between drive systems and local area network (LAN) protocols. GFK-0728A shows an interface between a drive and a LAN (Figure 2, on page 3, shows a labeled drawing of the module). Although GFK-0728A shows substantial features of the claimed invention, GFK-0728A is silent as to the specific circuitry of the interface module. Nonetheless the circuitry for interfacing a drive to a LAN is well known in the art and would have been an obvious modification to the system disclosed by GFK-0728A as evidenced by Kerr.

In analogous art, Kerr discloses data transfer circuitry that could be used to implement the system of GFK-0728A. In referring to claims 1, 8, and 15, Kerr shows,

- A dual port memory connected to a bus:
  GFK-0728A, col. 3, lines 39-45 (see full quote above)
- An ASIC:
  "The digital signal processor with an ASIC wrapper of this invention together provide super-bus-mastering to access the entire memory space in the system, including the entire virtual memory space accessible by the host processor." (GFK-0728A, col. 3, lines 49-53)
- An interrupt line:
  GFK-0728A, col. 5, lines 51-53 (see full quote above)
- Control registers:
  GFK-0728A, col. 6, lines 17-21 (see full quote above)

Given these teachings, a person of ordinary skill in the art would have readily recognized the desirability and advantages of using the data transfer circuitry of Kerr to

implement the system of GFK-0728A, in order to permit drives to be controlled from application programs.

In referring to claims 2 and 9, although GFK-0728A in view of Kerr shows substantial features of the claimed invention, GFK-0728A in view of Kerr does not show the ASIC is a controller for interfacing with firmware in the communication processor in order to pass data between a main processor and the interface card. Nonetheless this feature is well known in the art and would have been an obvious implementation of the system disclosed by GFK-0728A in view of Kerr.

GFK-0728A shows an interface module that interfaces a LAN with a drive. A person of ordinary skill in the art would have readily recognized the desirability and advantages of implementing the system of GFK-0728A in view of Kerr so as to use the ASIC as a controller for interfacing with firmware in the communication processor in order to pass data between a main processor and the interface card, in order to allow the interface module to communicate with the drive.

Claims 3-5 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over GFK-0728A in view of Kerr in further view of GEI-100216 (Drive Control / LAN Communications Board DS200LDCC, May 1997, hereinafter "GEI-100216").

In referring to claims 3 and 10, although GFK-0728A in view of Kerr shows substantial features of the claimed invention, GFK-0728A in view of Kerr does not explicitly show a stab terminal, a LNPL connector, a 2PL connector or an AC/DC2000 drive. Nonetheless these features are well known in the art and would have been obvious modifications to the system disclosed by GFK-0728A in view of Kerr as evidenced by GEI-100216.

In analogous art, GEI-100216 discloses a stab terminal for a ground connection (page 3, column 2, "The LDCC includes a stab connection, COM1 (see Figure1) for use in high

noise environments when the common reference to the LAN interface boards needs stiffening.")

Given these teachings, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the interface card of GFK-0728A in view of Kerr so as to include a stab connector for ground, such as taught by GEI-100216, in order to adequately ground the drive.

In referring to claims 4 and 11, although GFK-0728A in view of Kerr shows substantial features of the claimed invention, GFK-0728A in view of Kerr does not explicitly show a stab terminal, a LNPL connector, a 2PL connector or an AC/DC2000 drive. Nonetheless these features are well known in the art and would have been obvious modifications to the system disclosed by GFK-0728A in view of Kerr as evidenced by GEI-100216.

In analogous art, GEI-100216 discloses a LNPL connector for connecting the interface card with the main control card of the drive (page 13, table 13, shows a "Connector LNPL, Ribbon Cable Connection to Genius/CPL Bus Interface Board")

Given these teachings, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the interface card of GFK-0728A in view of Kerr so as to, include a LNPL connector for data, such as taught by GEI-100216, in order to communicate with the main control card of the drive by utilizing the pre-existing connectors on the drive (i.e. without using an adapter).

In referring to claims 5 and 12, although GFK-0728A in view of Kerr shows substantial features of the claimed invention, GFK-0728A in view of Kerr does not explicitly show a stab terminal, a LNPL connector, a 2PL connector or an AC/DC2000 drive. Nonetheless these features are well known in the art and would have been obvious modifications to the system disclosed by GFK-0728A in view of Kerr as evidenced by GEI-100216.

In analogous art, GEI-100216 discloses a 2PL connector for transmitting power to the interface card (page 8, table 4, shows a "Connector 2PL, Power Cable Connection to Signal-Level Power Supply Board")

Given these teachings, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the interface card of GFK-0728A in view of Kerr so as to, include a 2PL connector, such as taught by GEI-100216, in order to power the interface card.

Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over GFK-0728A in view of Kerr and in further view of GEH-6380 (Installation Guidance for Innovation Series Drive Systems, 30 June 1999, hereinafter "GEH-6380").

In referring to claims 7 and 14, although GFK-0728A in view of Kerr shows substantial features of the claimed invention, GFK-0728A in view of Kerr does not explicitly show the LAN is an ISBus LAN. Nonetheless this feature is well known in the art and would have been an obvious modification to the system disclosed by GFK-0728A in view of Kerr as evidenced by GEH-638.

In analogous art, GEH-638 discloses a module that connects a drive to an ISBus LAN. GEH-638 shows the LAN is and ISBus LAN, (Figure 8-1 on page 8-2 shows, "Examples of Innovation Series Drive System Configuration Using ISBus")

Given these teachings, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the interface card of GFK-0728A in view of Kerr so as to connect to an ISBus LAN, such as taught by GEH-638, in order to provide "tight synchronous coupling between different devices in the system" (page 8-1, column 2).

Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over GFK-0728A in view of Kerr in view of Dye et al. (U.S. Patent Number 6,523,102, hereinafter "Dye").

In referring to claims 16-19, although GFK-0728A in view of Kerr shows substantial features of the claimed invention, GFK-0728A in view of Kerr does not explicitly show the steps of performing a page swap in memory after updating the feedbacks, storing the transmitted setpoints in an external RAM inactive page, and performing an external RAM page swap. Nonetheless these steps are well known in the art and would have been an obvious modification to the system disclosed by GFK-0728A in view of Kerr as evidenced by Dye.

In analogous art, Dye discloses prior art memory systems. Dye shows using active and inactive pages of memory to store data, and swapping said memory to and from an active page to an inactive page (column 2, lines 61-67 "An active page may be defined as an area or page of memory, typically 4096 bytes, which is actively used by the CPU during application execution. Active pages reside between or within system memory or CPU cache memory. An inactive page may be defined as an area or page of memory, typically 4096 bytes, which is not directly accessed by the CPU for application execution. Inactive pages may reside in the system memory, or may be stored locally or on networks on storage media such as disks. The page fault boundary 232 is dynamically allocated during run time operation to provide the best performance and operation as defined by many industry standard algorithms such as the LRU/LFU lazy replacement algorithm for page swapping to disk.")

Given these teachings, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the system of GFK-0728A in view of Kerr so as to store memory in inactive and active pages, such as taught by Dye, in order to free memory that is no longer in use, to avoid over-committing the memory.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott M. Klinger whose telephone number is (703) 305-8285. The examiner can normally be reached on M-F 7:00am - 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenn Burgess can be reached on (703) 305-4792. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Scott M. Klinger
Examiner
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